88F5182

Feroceon® Storage Networking SoC

Functional Errata, Interface Guidelines, and Restrictions

Doc. No. MV-S500802-00, Rev. E
April 29, 2008, Preliminary

Document Conventions

	**Note:** Provides related information or information of special importance.
	**Caution:** Indicates potential damage to hardware or software, or loss of data.
	**Warning:** Indicates a risk of personal injury.

Document Status

Doc Status: Preliminary	Technical Publication: 0.01

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Summary List of Guidelines and Restrictions

1. Introduction

This document provides details about identified functional errata, interface guidelines, and restrictions for the 88F5182-A1/A2 device.

Note The term “device” is used in this document to refer to the 88F5182.

1.1 Document Organization

This document is organized as follows:

- Section 2. "Revision History Table"
- Section 3. "Detailed Descriptions for Functional Errata" on page 14
- Section 4. "Detailed Descriptions for Guidelines and Restrictions" on page 24

1.2 Document Conventions

The title naming conventions for the Functional Errata, Interface Guidelines, and Restrictions use the following prefixes:

FE:	Functional Erratum
RM:	Register Misconfiguration
RES:	Restriction
GL:	Guideline

The following abbreviations are defined in the title name to indicate the related interface, feature, or unit:

CPU	CPU Interface
CESA	Cryptographic Engine and Security Accelerator
Dev	Device Controller
ETH	Gigabit Ethernet Controller
MEM	DDR SDRAM Controller
PCI	PCI Interface
PCIe	PCI Express Interface
SATA	Serial-ATA Interface
USB	USB 2.0 Interface

1.3 Related Documentation

Refer to the following documents for further product information.

- *88F5182 Feroceon® Storage Networking SoC User Manual*, Doc. No. MV-S103345-01
- *88F5182 Feroceon® Storage Networking SoC Datasheet*, Doc. No. MV-S103345-00
- *Orion SoC Hardware Design Guide,* Doc. No. MV-S103315-00[1]

1. This document is a Marvell proprietary confidential document requiring an NDA and can be downloaded from the Marvell Extranet.

2. Revision History Table

Table 1 details the document revision changes. These changes indicate whether any new errata, guidelines, or restrictions were identified, modified, or fixed in a given device revision.

Table 1: Document Revision History Table

Doc Rev #	Date	Devices Covered
Rev. A	**November 9, 2005**	**88F5182-A0**
First Errata Release		
Rev. B	**March 7, 2006**	**88F5182-A1/A2**
1. Added the following errata: • In Full Speed (FS) and Low Speed (LS) Modes Bus May Be Driven During Idle State on page 22 • First Symbol of SYNC Pattern May Be Longer than 1 Bit Time in High Speed (HS) Mode on page 22 • Wrong Key Is Calculated when Using the AES Decryption Engine on page 15 • Authentication with Fragment Data Mode on page 15 • Erroneous Result when Performing a Combined Operation on a Fragmented Frame on page 16 2 Move the following errata to the *88F5182 Interface Guidelines and Restrictions* (Doc. No. MV-S500803-00): • Wrong Default Value to PHY Mode 4 Register Bits[1:0] (FEr# SATA-S10) 3 Deleted the following errata since they are not relevant to this device: • PCI Ordering Is Not Maintained by the PCI Slave (FEr# PCI-P10) • Basic DMA Read Operation Requires ComChannel Bit Set to Read Data From a Hard Drive (FEr# SATA-S17) • Wrong EDMA Request Queue Out Pointer Address (FEr# SATA-S18) • Wrong EDMA Response Queue In Pointer Address (FEr# SATA-S19) • Assertion of the SERV Bit Without a Pending Command by the Hard Drive May Cause Command Completion With Error (FEr# SATA-S20)		
Rev. C	**January 15, 2008**	**88F5182-A1/A2**
1. Document reformatted and integrated the guidelines and restrictions from *88F5182 Feroceon® SOC Interface Guidelines and Restrictions* (Doc. No. MV-S300803-00 Rev. B). 2 Added the following errata: • PCI Express Port Hangs on Recovery During L1 State on page 17 • Received IntA/B/C/D Indication Not Cleared upon Link Down on page 17 • The Spread-Spectrum Modulation Frequency Fails on the Lower Boundary on page 19 • Avoiding Underrun when Working in Device HS Mode on page 23 3 Deleted the following errata since it is not relevant to this device: • DRQ Block Size Larger than or Equal to 4 KByte in a Write Multiple PIO Command Is Not Supported (FEr# SATA-S14)		

Table 1: Document Revision History Table (Continued)

Doc Rev #	Date	Devices Covered
4 Added the following guidelines: • MPU Enabling Order on page 25, • Clearing the IDMA Interrupts when the Cryptographic Engine and Security Accelerator is Working in Enhanced Mode on page 28 • GE_RXERR Signal Needs an External Pull-down on page 31. • PCI Express Address Window Mapping Mechanism as an Endpoint Device on page 35 • Addr64 Field in the PCI MSI Message Control Register Has No Effect on page 37 • Using SATA II 3.0 Gbps Host with 1.5 Gbps Device on page 41 • PHY Mode 1 Register Configuration on page 41 • USB Full Speed—Receiving Packets with No EOP Indication on page 46 • USB High Speed—Receiving Packets with No EOP Indication on page 46 5 Added the following restriction: • PLD Instruction Concurrent with CP15 Access on page 27 • In MPU Mode, Consecutive Accesses to CP14 May Hang the CPU on page 27 • Violating the PCI Express Compliance Test 1.7 Advance Error Reporting on page 36 6 Revised the following guidelines: • ICE-debugger Fails to Initialize when All Instructions Fetched Are Conditional False or Unsupported on page 24 • Working with Interrupt Coalescing on page 31. • Vbus Support through GPIO on page 43 • Avoiding Three Consecutive CRC Errors on the USB Port when Working in HS Mode on page 44 7 Revised the following restrictions: • Vector Catching of Reset Routine Is Not Supported on page 26 • USB Isochronous Mode on page 47		
Rev. D	**February 12, 2008**	**88F5182-A1/A2**
1. Added the following errata: • Error During Prefetch Abort Exception on page 14		
Rev. E	**April 29, 2008**	**88F5182-A1/A2**
Changed document classification.		

3. Detailed Descriptions for Functional Errata

This section provides detailed descriptions for each functional erratum. This includes detailed information about the fixed status of each erratum for the device revisions. In addition, the descriptions provide information about the availability of a workaround.

CPU Interface Errata

3.1 Error During Prefetch Abort Exception

Type: Functional Erratum
Ref #: FE-CPU-140
Relevant for: 88F5182-A1/A2

Description

If the CPU fetches code in the instruction space that has not been mapped in the Memory Management Unit (MMU), a prefetch abort exception is triggered. When this exception enters the Prefetch Abort exception handler, the Link register (R14_abt) may be erroneously advanced by an additional instruction address.

This erratum only occurs when both of the following conditions are met:

- The instruction fetch, from the unmapped virtual address in the MMU, is mapped to an I-cache entry that already contains an “ldrd” opcode pattern, with a base register (Rn) update.
- The commands pipeline contains four commands and the “ldrd” opcode pattern, with a base register (Rn) update, is the fifth command to enter the pipeline.

The Link register value is used to return to the original program at the end of the Prefetch Abort exception handler. Since the Link register value may be incorrectly advanced, the original instruction address (that caused the Prefetch Abort exception) is skipped when exiting from the Prefetch Abort exception handler.

Workaround

A compiler needs to include the following configuration details:

- Do not use an “ldrd” instruction in the code.
- The data structure (literal pool space) cannot be located at the same cache line as the instruction. It may contain a data pattern that is similar to “ldrd” instruction.
- A dummy instruction that branches to itself must be added between the last real instruction and the first data that belongs to the literal pool space..

Note

- This erratum scenario is very unlikely to occur, especially if the “ldrd” instruction is not used. Therefore, no action needs to be taken into consideration. However, if this erratum occurs during the code QA process, a minor change in the source code and recompilation solves the issue in most instances.
- Using the Marvell® SDK prevents "ldrd" commands in the compiled code. This SDK includes the GCC 3.4.4 compiler, with the default compilation flag: “–march=armv5t”.

Fix

This erratum may be fixed in future stepping of the device.

Cryptographic Engine and Security Accelerator Errata

3.2 Wrong Key Is Calculated when Using the AES Decryption Engine

Type: Functional Erratum
Ref #: FE-CESA-100
Relevant for: 88F5182-A1/A2

Description
The generated key may be incorrect, when the AES decrypting engine is activated, to calculate the AES decrypting key, by setting the AES Decryption Command register (offset: 0x9DDF0) <AesDecMakeKey> field (bit [2]) to 0x1.

Workaround
Use either option:

- When writing the keys for the AES Decryption engine (AES Decryption Key Column 0..7 registers, offsets: 0x9DDC0–0x9DDDC) before activating the key generation process, write the first key twice.

  OR

- Calculate the AES decryption key using the software.

Fix
This erratum may be fixed in a future revision of the device.

3.3 Authentication with Fragment Data Mode

Type: Functional Erratum
Ref #: FE-CESA-110
Relevant for: 88F5182-A1/A2

Description
The accelerator authentication operation result on the last fragmented section is incorrect when the Security Accelerator is set to:

- Authentication only. The Operation field is set to Authentication only mode (Security Accelerator Data Structure DWORD 0 bits [1:0] = 0x0).

  AND

- The data in the SRAM is fragmented. The <FragMode> field is not 0x0 (Security Accelerator Data Structure DWORD 0 bits [31:30] =0x0).

Workaround

- For HMAC Mode: HMAC-MD5 and HMAC-SHA1 algorithms activate the Security Accelerator in Fragment mode for the first and (if necessary) middle fragment(s). Read the temporary digest result from the SHA-1/MD5 Initial Value/Digest A-E register (offsets: 0x9DD00–0x9DD10) and complete the digest calculation of the Last fragment by the software.
- For non HMAC Mode: MD5 and SHA1 algorithms activate the Security Accelerator in Fragment mode for the first fragment only. After that operation is completed, read the temporary digest result from the SHA-1/MD5 Initial Value/Digest A–E register and complete the digest calculation for the rest of the data in the packet by the software.

Fix
This erratum may be fixed in a future revision of the device.

3.4 Erroneous Result when Performing a Combined Operation on a Fragmented Frame

Type: Functional Erratum
Ref #: FE-CESA-120
Relevant for: 88F5182-A1/A2

Description

When the Security Accelerator preforms a combined operation (Encryption/Decryption) on a fragmented frame, the result is wrong.

Fragment mode for combined operation is defined by the following data structure DWORD0 values:

Bits[31:30] are other than 0x0, and bits[1:0] equal 0x2 or 0x3.

Workaround

For Fragment mode combined operation only:

- If the operation is Encryption/Decryption and then Authentication, perform only an Encryption/Decryption operation on the packet first. Following this first operation, perform the Authentication operation on the result.
- If the operation is Authentication and then Encryption/Decryption, perform only an Authentication operation on the packet first. Following this first operation, perform an Encryption/Decryption operation on the result.

Fix

This erratum may be fixed in a future revision of the device.

Gigabit Ethernet Controller Errata

3.5 Wrong Values in MIB Counter

Type: Functional Erratum
Ref #: FE-ETH-100
Relevant for: 88F5182-A1/A2

Description

The following MIB counters are incremented because of Tx Flow Control frames sent from the Ethernet port:

- MIB counter 13—GoodOctetsSent (the sum of lengths of all good Ethernet octets sent from this MAC)
- MIB counter 14—GoodFramesSent (the number of Ethernet frames sent from this MAC)
- MIB counter 16—MulticastFramesSent
- MIB counter 17—BroadcastFramesSent

Workaround

None.

Fix

This erratum may be fixed in a future revision of the device.

3.6 Collision During Preamble or Start Frame Delimiter (SFD)

Type: Functional Erratum
Ref #: FE-ETH-110
Relevant for: 88F5182-A1/A2

Description
When a collision occurs during frame transmission (by the MAC) of the preamble or SFD, the Gigabit MAC (Tx) operates incorrectly. In this case, the MAC must complete transmission of the preamble, SFD (preamble + SFD = 64 BT) and a 32-BT (Bit Time) jam pattern.

The MAC will transmit a 32+64=96 BT but without transmission of the SFD. The jam pattern exceeds 32 BT and is transmitted instead of the SFD.

Workaround
None.

Fix
This erratum may be fixed in a future revision of the device.

PCI Express Interface Errata

3.7 PCI Express Port Hangs on Recovery During L1 State

Type: Functional Erratum
Ref #: FE-PCIe-10
Relevant for: 88F5182-A1/A2

Description
If the LTSSM moves to Recovery when in L1 state, the L1 indication is lost, and the L1 process is not executed properly. This may cause the PCI Express port to hang.

Workaround
Do not use Power Management states (Dstates).

Fix
This erratum may be fixed in a future revision of the device.

3.8 Received IntA/B/C/D Indication Not Cleared upon Link Down

Type: Functional Erratum
Ref #: FE-PCIe-20
Relevant for: 88F5182-A1/A2

Description
The received IntA/B/C/D indication in the PCI Express interrupt Cause register is not cleared upon link down. This may cause a false interrupt when the link goes up again.

Workaround
Clear RcvIntA/B/C/D bits upon link down.

Fix
This erratum may be fixed in a future revision of the device.

Serial-ATA Interface Errata

3.9 Support in PIO Data-in/Data-out Commands Is Restricted to a Single DRQ

Type: Functional Erratum
Ref #: FE-SATA-160
Relevant for: 88F5182-A1/A2

Description

The Device - Command/Status register and Device - Control/Alternate Status register —in the ATA shadow registers— may not hold the updated status when there is more than one DRQ in a PIO data-in/data-out command.

The offsets of the Device - Command/Status register are:

- Port 0: 0x8211C
- Port 1: 0x8411C

The offsets of the Device - Control/Alternate Status register are:

- Port 0: 0x82120
- Port 1: 0x84120

Workaround

To ensure that there is only one DSQ in the PIO data-in/data-out command:

1. Prior to executing the Read/Write command to the disk, the host must enable the storage device interrupts (set <nIEN> bit[1] to 0 in the Device - Control/Alternate Status register).
2. After each DRQ write or read, the host must wait for the assertion (to 1) of the interrupt that comes from the device (<SaDevInterruptn> bit[8], [9], [10], [11] in the SATAHC Interrupt Cause register, offset: SATAHC0 0x80014).
3. Before continuing to the next DRQ, the host clears the interrupt, waits for the BUSY bit to clear, and waits for the DRQ bit to be set.

Fix

This erratum may be fixed in a future revision of the device.

3.10 HOB Bit Does Not Clear by Writing to Any Command Block Register

Type: Functional Erratum
Ref #: FE-SATA-180
Relevant for: 88F5182-A1/A2

Description

The 48-bit address feature set defines the High Order Byte (HOB). In the Device - Control/Alternate Status register—in the ATA shadow registers—a write to any Command Block register does not clear <HOB> bit[7], as it should.

Workaround

The only way to clear this bit is a direct write to the Device Control/Alternate Status register.

Fix

This erratum may be fixed in a future revision of the device.

3.11 Inconsistent Operation of Rx Impedance Auto-calibration

Type: Functional Erratum
Ref #: FE-SATA-230
Relevant for: 88F5182-A1/A2

Description
After power up or hard reset, the Rx impedance auto-calibration does not always work. When Rx impedance auto-calibration is not working, the value 0xF is read from the PHY Mode 2 register bits[29:26].

Workaround
Bit[31] in the PHY Mode 2 register initiates the auto-calibration. To modify the register, a flow of read-modify-write is performed to avoid overriding other bits in the register. After hardware reset or ATA reset, restart the Rx impedance auto-calibration as follows:

1. Delay the loop for at least 200 µs (1k cycles), the time needed for the auto-calibration to finish.
2. Read the PHY Mode 2 register of all ports.
3. Set the Impedance Calibration Enable bit[31] and clear (write 0) bit[16], in the PHY Mode 2 register, and update the register.
4. Delay the loop for at least 200 µs.
5. Read the PHY Mode 2 register, and confirm that the value of bits[29:26] is a value other than 0xF.
6. Clear bit[31] in the PHY Mode 2 register, and update the register.
7. Before issuing any other SATA command, delay the loop for at least 200 µs.

Fix
This erratum may be fixed in a future revision of the device.

3.12 The Spread-Spectrum Modulation Frequency Fails on the Lower Boundary

Type: Functional Erratum
Ref #: FE-SATA-250
Relevant for: 88F5182

Description
Although the SATA specification states that the f_{SSC} measurement should be between 30–33 kHz, this measurement starts from 29.95 kHz (not 30 kHz), less than a 0.2% violation, in the 88F5182 device.

This minor violation should not influence the SATA Drive PHY because it is in the lower boundary frequency. The HD SATA Driver phase loop will lock on a lower modulation frequency.

Workaround
No workaround is required. There is no functional impact as a result of this minor violation.

Fix
There are no current plans to fix this erratum in a future revision of the device.

USB 2.0 Interface Errata

3.13 USB Host Compliance Electrical Test Plan—EL23

Type: Functional Erratum
Ref #: FE-USB-100
Relevant for: 88F5182-A1

Description

Hosts transmitting two packets in a row must have an interpacket gap of at least 88 bit times and not more than 192 bit times.

The device USB controller supports an interpacket gap of at least 40 bit times, which does not comply with the USB host specification.

Note

See Enable Fix for USB Host Compliance Electrical Test Plan-EL23-Errata FEr# USB-U10 (GL# USB-10) in the *88F5182 Interface Guidelines and Restrictions*.

Workaround

None.

Fix

This erratum was fixed in revision 88F5182-A2 of the device.

3.14 USB Electrical Test Plan EL24

Type: Functional Erratum
Ref #: FE-USB-110
Relevant for: 88F5182-A1/A2

Description

A host or device expecting a response to a transmission must *not* timeout the transaction if the interpacket delay is less than 736 bit times, and it must timeout the transaction if no signaling is seen within 816 bit times.

The device's USB controller allows for a longer delay than 816 bit times. It allows for an additional 1.5us (above the 816 bit times).

This was done because many high speed devices are not able to respond within 816 bit times. Therefore, it was necessary to increase the allowed timing window, to permit interoperability with other devices from other vendors.

EL24 is not part of compliance requirements, but is part of the USB Electrical Test Plan (ETP).

Workaround

None.

Fix

This erratum may be fixed in a future revision of the device.

3.15 Response to Split Interrupt Transfer Triggers Immediate Retry

Type: Functional Erratum
Ref #: FE-USB-120
Relevant for: 88F5182-A1/A2

Description
A host response to an MDATA handshake response, which results from a split-Interrupt transfer on the last of the c-mask bits, is noted in the QH/qTD as a transfer error, and an immediate retry is initiated.

Workaround
None.

Fix
This erratum may be fixed in a future revision of the device.

3.16 Missed Micro-frame Detection is not Indicated in Host Mode

Type: Functional Erratum
Ref #: FE-USB-130
Relevant for: 88F5182-A1/A2

Description
While processing a split-interrupt transaction, a missed micro-frame is not detected when the QH SMASK bit is set for the current micro-frame, and the QH split state is set for completion.

Workaround
None.

Fix
This erratum may be fixed in a future revision of the device.

3.17 Byte-only Writes to the NAK Detection Register Fail in Device Mode

Type: Functional Erratum
Ref #: FE-USB-140
Relevant for: 88F5182-A1/A2

Description
Byte-only writes to the ENDPTNAK Detection register (offset: 0xA0178, 0x50178) do not operate properly.

Workaround
Use only word and long word writes to the ENDPTNAK Detection register.

Fix
This erratum may be fixed in a future revision of the device.

3.18 SOF Transmitted in TEST_MODE_SE0—Host Mode

Type: Functional Erratum
Ref #: FE-USB-150
Relevant for: 88F5182-A1/A2

Description
When in TEST_MODE_SE0 mode, the device erroneously sends packet start of frame (SOF) traffic.

Workaround
None.

Fix
This erratum may be fixed in a future revision of the device.

3.19 In Full Speed (FS) and Low Speed (LS) Modes Bus May Be Driven During Idle State

Type: Functional Erratum
Ref #: FE-USB-180
Relevant for: 88F5182-A1/A2

Description

While working in Full Speed (FS) mode or in Low Speed (LS) mode, the USB PHY may drive the bus during Idle state, under the following conditions:

- End-of-Packet (EOP) is indicated by SE0 state for two bit times, followed by J state for one bit time (i.e., 83.36 ns in FS mode), and then turn to Idle state. Instead, the device USB PHY extends the J state up to 116 ns in FS mode and 703 ns in LS mode, before returning to Idle state.
- Start-of-Packet (SOP) is signaled by driving the bus from the Idle state to K state. This represents the first bit of a SYNC pattern. The PHY should start a SYNC pattern directly from an Idle state. Instead, the device USB PHY drives J state for approximately 232 ns in FS mode and 1300 ns in LS mode, before driving the first bit of a SYNC pattern.

In both cases, the device USB PHY drives J state, when the bus should be in Idle state.

Workaround

None.

There is no workaround since when working in FS mode or LS mode, Idle state and J state have the same logic value at the receiver, and therefore, a USB receiver is unaware of whether the bus is driven to J state or Idle state.

Fix

This erratum may be fixed in a future revision of the device.

3.20 First Symbol of SYNC Pattern May Be Longer than 1 Bit Time in High Speed (HS) Mode

Type: Functional Erratum
Ref #: FE-USB-190
Relevant for: 88F5182-A1/A2

Description

The first symbol of a SYNC pattern in High Speed mode should be a K state for 2 ns (one bit time). However, the device USB PHY drives the first SYNC pattern K state for a duration of 3.5 ns.

Workaround

None.

There is no workaround since the first symbol of the SYNC pattern is used by the receiver for squelch detection only (not for clock recovery), and therefore the duration of the first symbol would not effect the normal receiver behavior.

Fix

This erratum may be fixed in a future revision of the device.

3.21 Avoiding Underrun when Working in Device HS Mode

Type: Functional Erratum
Ref #: FE-USB-200
Relevant for: 88F5182-A1/A2

Description

When working in HS Device mode, an underrun may occur, if a packet size is larger than 128 bytes. The underrun is due to high latency DDR-DRAM transactions.

This underrun causes a CRC error, which is detected by the Host.

Workaround

Set the USBMODE register (offset 0x501A8) bit[4] to 1, which activates Stream Disable mode.

- When working in Device mode and not using Bulk Endpoint transfer, restrict the maximum packet size used by the device to 128 bytes.
- When working in Device mode and using Bulk Endpoint, use an IDMA to copy up to 4 KByte of the data from the DDR-DRAM to a fast internal SRAM (at default the base address is 0xC801.0000). This causes the USB unit to read the data from the internal SRAM and not from the external DDR-DRAM.

Fix

This erratum may be fixed in a future revision of the device.

4. Detailed Descriptions for Guidelines and Restrictions

This section provides detailed guidelines and lists restrictions.

CPU Interface Guidelines

4.1 ICE-debugger Fails to Initialize when All Instructions Fetched Are Conditional False or Unsupported

Type: Guideline
Ref #: GL-CPU-10
Relevant for: 88F5182-A1/A2

Description

ICE-debugger may take control only after at least one command retires from the execution unit.

When the boot address space contains only conditional false instructions or unsupported instructions[1], these instructions do not enter the execution unit, and therefore, are never retired.

Since there is no execution-retirement, the debugger never gains control of the CPU and, therefore, hangs.

Steps to be performed by the designer

Option 1:

Connect the SRST coming from the JTAG connector to the SYSRSTn going into the device.

Make sure the instruction resides in a boot address space that is valid and conditional true.

Option 2:

Connect the SRST coming from the JTAG connector to the SYSRSTn going into the device.

Add to the board options for:

- A TWSI EEPROM
- Ability to connect an external SEEPROM to signals SDL, SDC, GND, and 3.3V.

Configure the board to enable SEEPROM initialization in the reset configuration.

Use the serial ROM to change the boot location and the boot vector. Change the boot vector to 0x0, and set the PCI so that it is not in master enabled mode. The address 0x0 is mapped to the PCI memory space region.

After the CPU reset is de-asserted, it fetches boot instructions from the PCI, which returns a value 0xFFFFFFFF (since the master is disabled). The value 0xFFFFFFFF is defined as a conditional true instruction, allowing the debugger to take control of the CPU.

To configure this setup, the Serial ROM needs to contain the following data:

Table 2: Serial ROM Initialization Data

Address	Data	Comment
0xD0020100	0x00000001	VECInit = 0
0xD0020014	0x00000000	PCI win base = 0x0
0xD0001504	0x00000000	DDR CS0 win disable
0xFFFFFFFF	0xFFFFFFFF	

For the TWSI initialization feature, refer to the Serial ROM Initialization section in the datasheet.

1. These are instructions that are neither defined nor undefined, as described in the *ARM Architect Reference Manual*, Second Edition.

4.2 IDCODE of the CPU Should Be Ignored

Type: Guideline
Ref #: GL-CPU-20
Relevant for: 88F5182-A1/A2

Description
When the JTAG IDCODE instruction is executed, the JTAG tap controller returns an IDCODE that should be ignored by the designer.

Steps to be performed by the designer
If the Manufacturer ID, Part Number, and Revision ID are required, the designer can read them through the PCI or PCI Express ports (reading Function 0 configuration registers, offset:0x00 and offset 0x08, or reading the PCI Express Device and Vendor ID Register, offset: 0x40000).

4.3 MPU Enabling Order

Type: Guideline
Ref #: GL-CPU-30
Relevant for: 88F5182-A1/A2

Description
When enabling the MPU (Memory Protection Unit), always set the regions and permissions first and then set the Protection Unit Enable bit in CP15 Reg 1 (bit [0]), using the MCR command. This ensures that the configurations are set correctly and are ready to be used once the mode is enabled.

Steps to be performed by the designer
The MPU must be enabled in the following order;

1. Set the regions and their permissions.
2. Protection Unit enable bit.

CPU Interface Restrictions

4.4 Watch Points at Dual Retirement May Stop after the Second Command

Type: Restriction
Ref #: RES-CPU-10
Relevant for: 88F5182-A1/A2

Description
When setting a watch point, the break point normally occurs at the retirement time of the watched instruction.

When dual retirement occurs in the 88F5182 devices, it may be that with the watched instruction—a second instruction will retire, and the break point will account for both, leading to recovery of the next command in the instruction stream.

This is acceptable behavior, according to the *ARM Architecture Reference Manual*, Second Edition. There is no requirement for a firm stop point for a proposed watch point.

Workaround
The designer must be aware of this behavior, in case two consecutive commands that are retiring together, attempt to modify the same register.

4.5 ICE Vector Catch Register Is Not Initialized

Type: Restriction
Ref #: RES-CPU-20
Relevant for: 88F5182-A1/A2

Description
The Vector Catch register that informs the ICE for which event to watch, wakes up as not initialized after TAP reset. This may result in unexpected behavior once the ICE/Debugger is enabled.

Workaround
Prior to releasing the CPU reset, issue a debugger routine setting the Vector Catching register.

4.6 Vector Catching of Reset Routine Is Not Supported

Type: Restriction
Ref #: RES-CPU-30
Relevant for: 88F5182-A1/A2

Description
The JTAG ICE controller does not support vector catching of the reset routine.

Workaround
Use one of the following workarounds:

- Configure a break point on the reset vector (0xFFFF000 or 0x0).
- Manually insert an SWI instruction in the boot code.

4.7 ICE Method of Entry (MOE) Is Not Supported

Type: Restriction
Ref #: RES-CPU-40
Relevant for: 88F5182-A1/A2

Description
The Method of Entry (MOE), providing the reason for the break point that was used, is not implemented in the device's JTAG ICE controller.

Workaround
None.

4.8 WP/BP on Second Address/Data of Load/Store Double Instructions Is Ignored

Type: Restriction
Ref #: RES-CPU-50
Relevant for: 88F5182-A1/A2

Description
Watch points/break points (WP/BP) cannot be set on the second Address/Data of Load/Store double or multiple instructions.

Such watch points/break points are ignored and not caught.

Workaround
In Debug mode, avoid using break points on Load/Store double and Load/Store multiple instructions.

4.9 Exception Not Generated for LDRD/STRD Command Using a 4-byte Aligned Address

Type: Restriction
Ref #: RES-CPU-60
Relevant for: 88F5182-A1
Not Relevant for: 88F5182-A2

Description
The ARMv5TE manual (revision DDI0100E) requires the use of only an 8-byte aligned address for the Load Doubleword (LDRD) and Store Doubleword (STRD) commands. Use of a 4-byte aligned address for STRD/LDRD commands is not supported, and results in unpredictable data.

The ARMv5TE manual specifies that generation of a data alignment exception is *implementation dependent* in the case of a 4-byte aligned address. Other alignment errors, such as 2-bytes alignment, would generate a data alignment exception.

The 88F5182 device does not generate data alignment exception in the case of a 4-byte aligned address. However, to aid program debug, in case of using LDRD/STRD with 4-byte alignment, a data alignment exception is desired. For devices that do not support data alignment exception in the described condition it is suggested to use the following workaround.

Workaround
The software designer should either:

- Ensure 8-byte alignment, as per the ARM EABI and the ARMv5TE specifications.

  OR
- If such alignment cannot be guaranteed, use compiler flags to prevent generation of the E-architecture extension (which includes the double-word load/store instructions).

4.10 In MPU Mode, Consecutive Accesses to CP14 May Hang the CPU

Type: Restriction
Ref #: RES-CPU-70
Relevant for: 88F5182-A1/A2

Description
In MPU mode, consecutive accesses to CP14 may hang the CPU.

Workaround
In MPU mode, make sure that two consecutive accesses to CP14 are always separated by a non-CP14 instructions. This eliminates the deadlock condition.

4.11 PLD Instruction Concurrent with CP15 Access

Type: Restriction
Ref #: RES-CPU-90
Relevant for: 88F5182-A1/A2

Description
When a CP15 and a PLD access occur concurrently, the PLD updates the cache line that corresponds to the CP15 access address, preventing access to CP15.

Steps to be preformed by the designer
Always insert a Load/Store command into any address between the PLD and the MCR instructions. This causes the two accesses to occur sequentially, and avoids the conflicting accesses.

Fix
None.

Cryptographic Engine and Security Accelerator Guidelines

4.12 Clearing the Cryptographic Engines and Security Accelerator Interrupt Cause Register

Type: Guideline
Ref #: GL-CESA-100
Relevant for: 88F5182-A1/A2

Description

Writing 0 to bits[6:0] of the Cryptographic Engines and Security Accelerator Interrupt Cause register (offset 0x9DE20) has no effect.

Steps to be performed by the designer

Before writing 0 to any of the bits[6:0] of the Cryptographic Engines and Security Accelerator Interrupt Cause register, the software must write 0 to the corresponding bit of the internal register at offset 0x9DD68.

Writing to offset 0x9DD68 is not possible when any of the Security Accelerators' sessions are active. Therefore, the software must verify that no channel is active before clearing any of those interrupts.

4.13 Clearing the IDMA Interrupts when the Cryptographic Engine and Security Accelerator is Working in Enhanced Mode

Type: Guideline
Ref #: GL-CESA-110
Relevant for: 88F5182-A1/A2

Description

When the Cryptographic Engine and Security Accelerator is working in Enhanced mode, the Acceleration and IDMA Interrupt bits—<AccAndIDMAInt1/0> bits [8:7]—in the Cryptographic Engines and Security Accelerator Interrupt Cause register (offset: 0x9DE20) may be skipped.

Steps to be performed by the designer

Whenever the interrupt in the IDMA Interrupt Cause register (offset: 0x608C0) is cleared, only the relevant Byte Enable should be asserted.

For example, when clearing interrupt IDMA channel 0, write 0x0 to the relevant bit in the register with Byte Enable set to 4b1110, which updates byte 0 of this IDMA Interrupt Cause register.

Gigabit Ethernet Controller Guidelines

4.14 Switching Speed without Link Down

Type: Guideline
Ref #: GL-ETH-20
Relevant for: 88F5182-A1/A2

Description

False (not real) packets without CRC error indication are received when switching speed (bit rate) without link down. This situation may occur when both PHYs work without link and speed auto-negotiation (link is forced to link up). Therefore, the Gigabit Ethernet receive side will have no indication for link down or speed switching, and will erroneously work with the previous configured speed. This results in false incoming frames of different sizes (including fragmented frames) even if the far side did not send any frames after the speed switching.

Steps to be performed by the designer

When working without link and speed auto-negotiation, the Gigabit Ethernet link should be forced to link fail (down) before:

- Switching speed in the far side.
- Switching the Gigabit Ethernet speed configuration.

4.15 RGMII Output Delay Tuning

Type: Guideline
Ref #: GL-ETH-30
Relevant for: 88F5182-A1/A2

Description

When the Gigabit Ethernet port is configured to work in RGMII mode, the designer must configure a register at offset 0x104F0 as described below, to meet the timing parameter TskewT in the *88F5182 Datasheet*.

Steps to be performed by the designer

Use Read Modify Write to change bits[1:0] at offset 0x104F0 to 0x2.

4.16 Wrong Checksum Error on TCP/UDP with Empty Data Field

Type: Guideline
Ref #: GL-ETH-40
Relevant for: 88F5182-A1/A2

Description

The <L4ChkOK> bit[30] in the Receive Descriptor—Command/ Status register may erroneously be set when:

- Receiving TCP/UDP packets with a minimal TCP/UDP header of 5 DWORDs for TCP or 2 DWORDs for UDP (a DWORD is 4 bytes long).
- There is no data field after the TCP/UDP header. The IP layer ends at the end of the TCP/UDP header, and there is no data field in TCP/UDP layer.
- TCP/UDP data field does not contain any zero padding for a minimal Ethernet packet length.

Steps to be performed by the designer

When <L4ChkOK> is set, the software must check for TCP/UDP header lengths of 5DWORD/2DWORD and for no TCP/UDP data field after the TCP/UDP header (IP length equal to IP and TCP/UDP total header length).

If this condition is met, the checksum error indication must be manually calculated by the software, by calculating the TCP/UDP checksum and comparing it with the original receiving packet checksum field.

To cover all types of packets, it is recommended that any packet with sum of IP + TCP Headers + Descriptor's Byte Count field length of less than or equal to 72 bytes will have its checksum calculated manually (by the software) and compared with the original receiving packet checksum. This takes into account the worst scenario of IEEE 802.3 Ethernet LLC+SNAP+VLAN + IPv4+ TCP.

4.17 Wrong Tx TCP/UDP Checksum Generation

Type: Guideline
Ref #: GL-ETH-50
Relevant for: 88F5182-A1/A2

Description

The TCP/UDP checksum of the transmitted packet will not be generated correctly when the previous packet had a first descriptor with the <IPV4HdLen> field equal to 0x0.

Steps to be performed by the designer

Set the <IPV4HdLen> field to 0x5 for every first Tx descriptor (bit[21] of the command/status set to 1) that does not generate an IP or TCP/UDP checksum (bits[17] and [18] of the command/status are set to 0).

For the Tx first descriptor whose IP or TCP/UDP checksum bits are set to 1, the <IPV4HdLen> field value should be set to a valid value of 5–15.

4.18 Working with Interrupt Coalescing

Type: Guideline
Ref #: GL-ETH-60
Relevant for: 88F5182-A1/A2

Description

The synchronization between the Port Interrupt Cause register (PICR) or the Port Interrupt Cause Extended register (PICER) and the device internal shadow register may fail under any of the following circumstances:

- If the CPU reads either of these cause registers before the coalescing Tx/Rx countdown timer expires, the contents of the shadow register are cleared and it begins to accumulate new interrupts. When the counter expires, the contents of the shadow register overwrites the cause register. For example, bits set in the cause register, prior to the CPU read, may be cleared when the countdown timer expires, and the shadow register's contents are copied to the cause register.
- If a new interrupt is generated simultaneously with the CPU reading either of the cause registers, the interrupt may not be recorded.
- If a new interrupt is generated simultaneously with the countdown timer expiration, the interrupt may not be recorded. Normally, the interrupt coalescing mechanism is used from the point when the CPU reads the PICR or the PICER. The interrupts are stored in a shadow register. When the coalescing countdown ends, these interrupts are copied to the PICR and PICER.
- If a new interrupt is generated simultaneously with the CPU clearing (writing 0) the interrupt cause bit, the new interrupt can be registered in the cause register and in the shadow register. As a result, the interrupt would be reported twice.

Steps to be performed by the designer

When using the interrupt coalescing mechanism, implement the following workarounds:

- To avoid the cause register override scenario (the first bullet above), the ISR must read the cause register once and hold a copy of it for later use.
- For cases in which the new interrupt is generated simultaneously with the CPU reading a cause registers (the second bullet above), or generated simultaneously with the countdown timer expiration (the third bullet above), use a system timer (e.g., the CPU Timer 0) to periodically interrupt the CPU. This interrupt service routine checks the active queues for packet descriptors that were handled by the Ethernet unit without the CPU being notified.
- For cases where two interrupts are generated (the fourth bullet above), no action is required. Since the CPU finds that the queues are empty, it exits the interrupt routine.

4.19 GE_RXERR Signal Needs an External Pull-down

Type: Guideline
Ref #: GL-ETH-70
Relevant for: 88F5182-A0/A1

Description

When the Gigabit Ethernet port works in GMII mode, the GE_RXERR signal must be driven by the system board, even if the signal functionality is not needed (i.e., when connecting MAC-to-MAC). Therefore, the MPP pin that is used for the GE_RXERR signal must be configured to GMII mode and be driven by the system board to 0 (see the *88F5182 Datasheet*).

The GE_CRS and GE_COL signals do not need to be driven, if forced to full duplex.

Steps to be performed by the designer

Perform both of the following steps:

1. In the MPP Control 1 Register (offset: 0x10004), set field <MPPSel9> (bits [7:4]) to 0x1 to configure the Gigabit Ethernet port to GMII mode.
   AND
2. On the system board, pull down the MPP pin used for the GE_RXERR signal.

Gigabit Ethernet Controller Restriction

4.20 Incorrect Tx L4 Checksum Calculation for a UDP Packet with an Empty L4 Data Field

Type: Restriction
Ref #: RES-ETH-10
Relevant for: 88F5182-A1/A2

Description

The Ethernet interface may calculate an incorrect L4 checksum when a UDP packet is transmitted with no L4 payload data (i.e., when the IP data payload includes only a UDP header).

Steps to be performed by the designer

For UDP packets with no L4 payload data, to calculate the UDP checksum correctly, the software must set the checksum field in the UDP header to 0x0000. This is in addition to setting the <GL4chk> bit[17] to 1, in the Transmit Descriptor—Command/Status word.

DDR SDRAM Controller Guidelines

4.21 ODT Signal is De-asserted Too Early in Self Refresh Mode

Type: Guideline
Ref #: GL-MEM-10
Relevant for: Orion-ALL-A0

Description

The On Die Termination (ODT), both in the controller and in the standby DIMM, might be turned off while receiving data from memory. This may cause an error.

This scenario may occur when one of the following conditions exists:

- CAS Latency <CL> field [6:4] in the DDR SDRAM Mode register (offset: 0x0141C) is set to 4 (for unbuffered DIMM).
- Registered DIMMs are used, and the <CL> is set to 3.

Steps to be performed by the designer

To avoid this scenario, make sure the ODT control signals are de-asserted 2.5 cycles before entering Self-Refresh mode. To accomplish this, do either of the following:

- When working with registered DIMMs and <CL> is set to 3, increase the value of <t_{RTP}> (field [31:28] in the DDR SDRAM Timing (Low) register, offset: 0x01408) by 1.
  OR
- Set the software to issue a self refresh command only when there are no pending transactions towards the SDRAM.

4.22 Drive Strength Value

Type: Guideline
Ref #: GL-MEM-30
Relevant for: 88F5182-A1/A2

Description

The <DriveStrength> default value DDR SDRAM Address/Control Pads Calibration register (offset: 0x014C0) and the DDR SDRAM Data Pads Calibration register (offset: 0x014C4) must be updated for DDR1 and DDR2 after reset by using a Read/Modify/Write operation.

Steps to be performed by the designer

Perform the following steps in both of the following registers:

- DDR SDRAM Address/Control Pads Calibration register
- DDR SDRAM Data Pads Calibration register

1. Set bit[31] to 1.
2. Update bits[13:12] <DriveStrength> to 3, when using DDR2, or to 1, when using DDR1,
3. Clear bit[31] to protect register content.

4.23 DQS Reference Delay Tuning

Type: Guideline
Ref #: GL-MEM-40
Relevant for: 88F5182-A1/A2

Description

The DQS reference delay must be manually tuned by the designer.

Steps to be performed by the designer

Perform the following steps:

1. Read DDR Timing Adjustment Register.
2. Set bit[0] to 1 to enable write.
3. Write the register value according to the following table. Ensure that bit[0] is set to 1.

	DDR1		DDR2		
Device	**133 MHz**	**166 MHz**	**133 MHz**	**166 MHz**	**200 MHz**
88F5182	0x47F000	0x45D000	0xF95000	0x597000	0xF95000
88F5082	0x47F000	0x45D000	0xF95000	n/a	n/a

4. Rewrite the register value from the table. Ensure that bit[0] is set to 0.

PCI Express Interface Guideline

4.24 Erroneous Read Data on Configuration Reads

Type: Guideline
Ref #: GL-PCIe-10
Relevant for: 88F5182-A1/A2

Description

If all of the following conditions exist, the data in the data register is incorrect:

- Configuration read accesses towards the PCI Express use the CF8/CFC mechanism (PCI Express Configuration Address register/PCI Express Configuration Data register, offset: 0x418F8/0x418FC).
- The configuration read access in not targeting the PCI Express port internal configuration registers (the bus number and/or device number are different form the internal bus and device numbers). In this case a configuration transaction will be transmitted on the PCI Express bus.
- The register address is DWORD aligned (0x418F8[2] = register_address[2] = 0).
- The address was written to the PCI Express Configuration Address register (offset: 0x418F8).
- Data was read from the PCI Express Configuration Data register (offset: 0x418FC).

Steps to be performed by the designer

- When the read is finished, read the PCI Express Header Log Fourth DWORD register (offset 0x40128). This is the Header Log register that holds the last received TLP fourth DWORD, which will hold the configuration read data.

  OR

- Use the peer-to-peer mechanism (i.e., direct configuration access mechanism).

4.25 Wrong Default Value to Transmitter Output Current (TXAMP)

Type: Guideline
Ref #: GL-PCIe-20
Relevant for: 88F5182-A1/A2

Description

To meet the PCI Express specification, the PCI Express Transmitter Output Current (TXAMP) default value of 3 must be changed to 4.

Steps to be performed by the designer

Perform the following sequence:

1. Write 0x80820000 to register offset 0x41B00.
2. Read register 0x41B00 (The relevant data is in bits[15:0]).
3. Write the data from the last read to offset 0x41B00 with bits[2:0] updated to 3’b100.

4.26 PCI Express Endpoint Hot Reset Duration

Type: Guideline
Ref #: GL-PCIe-30
Relevant for: 88F5182-A1/A2

Description

When the device works as a PCI Express Endpoint, a link fail and/or a hot reset indication triggers an internal reset signal in the device. All the device logic is reset to the default values, except for the sticky register bits and the sample on reset logic. In addition, the MPP[0] pin can be used as an external reset signal to reset other components on the system board. The duration of the internal reset is 6 µs.

If any external device requires a longer reset duration, the MPP[0] reset needs to be extended by external logic. In this case, the CPU may exit from reset state and access other components of the board that are still in a reset state. This may lead to system malfunction.

Steps to be performed by the designer

Perform either of the following options:

- Internally mask the PCI Express reset signal. The reset conditions also generate an interrupt to the CPU. The software interrupt handler can perform a controlled reset.
- Use a software delay before accessing any external devices that may have a longer reset period. The Two-Wire Serial Interface (TWSI) Serial EEPROM (SEEPROM) and the boot device are accessed before the software initiates the delay, therefore, these devices need not to be connected to the reset signal or have a reset period no longer then 6 µs.

4.27 PCI Express Address Window Mapping Mechanism as an Endpoint Device

Type: Guideline
Ref #: GL-PCIe-40
Relevant for: 88F5182-A1/A2

Description

In the PCI Express standard, the host may configure the Base Address Register (BAR) of a device in Endpoint (EP) mode after link initialization. The new mapping occurs after the Endpoint self configuration.

In Endpoint mode, three BARs (offsets: 0x40010, 0x40018, and 0x40020) allocate different areas in the memory address space. In addition, six PCI Express address windows define address space within the BARs space. Those windows are defined in another set of registers (offset: 0x41820–0x418C4).

When the host changes one of the BARs in the device in Endpoint mode, the PCI Express address windows will not be aligned with the new base address, and the mapping will be lost. In this case, the PCI Express address windows registers might be out of the BAR frame.

Steps to be performed by the designer

The PCI Express driver should poll the position of the BARs.

If one of the BARs has been changed, the driver should update the appropriate PCI Express address window register with the new values of the BAR.

PCI Express Interface Restrictions

4.28 Chip Hang on Disable or Hot Reset during L1

Type: Restriction
Ref #: RES-PCIe-10
Relevant for: 88F5182-A1/A2

Description

The PCI Express port may hang on an endless Recovery loop when:

- The 88F5182 PCI Express port is working in Root-complex mode
- AND
- The link is in L1 state, and directed by software to either Link Disable (bit[4] of the PCI Express Link Control Status register, offset: 0x40070) or Hot-reset mode (bit[24] of the PCI Express Control register, offset: 0x41A00)

Workaround

To avoid the described scenario, there are two options:

- Use Link Disable and Hot Reset only when the link is in L0 state.

  OR

- Do not use power management (Dstates).

s

4.29 Link Retrain Not Executed when Not in L0 State

Type: Restriction
Ref #: RES-PCIe-20
Relevant for: 88F5182-A1/A2

Description

If the software programs the PCI Express port to Link Disable mode (via bit[4] of the PCI Express Link Control Status register, offset: 0x40070), and the link is in L1 power management state, the Link Disable request is lost. The link will not transition to the disable state after it returns to L0 state.

Workaround

Use link Retrain only in L0 state.

4.30 Violating the PCI Express Compliance Test 1.7 Advance Error Reporting

Type: Restriction
Ref #: RES-PCIe-30
Relevant for: 88F5182-A1/A2

Description

The device violates the PCI Express Compliance Test 1.7 Advance Error Reporting due to writing to read only registers.

The relevant registers are:

- PCI Express Uncorrectable Error Mask Address register (offset: 0x40108)
- PCI Express Uncorrectable Error Severity Address register (offset: 0x4010C)
- PCI Express Uncorrectable Error Mask Address register (offset: 0x40114)

This violation has no impact on the functionality of the PCI Express port.

Workaround

None.

Since there is no impact in functionality, no action is necessary.

PCI Interface Guidelines

4.31 PCI Slave May Hang after Disconnecting an Aggressive Prefetch Read Transaction

Type: Guideline
Ref #: GL-PCI-10
Relevant for: 88F5182-A1/A2

Description

When the PCI slave disconnects an aggressive prefetch read transaction, it waits for the external PCI master to continue the read transaction from the point that it disconnected. While waiting for the transaction to continue, the PCI slave does not serve any other transaction, and the discard mechanism will not release the read buffers of the PCI slave, to continue serving other transactions.

Steps to be performed by the designer

The external PCI master must continue the read transaction from the point it was disconnected.

4.32 PCI May Respond to a Not Mapped PCI Address after Device Reset

Type: Guideline
Ref #: GL-PCI-20
Relevant for: 88F5182-A1/A2

Description

The PCI slave may erroneously respond to PCI memory read or write commands addressed to the PCI address range from 0x42000000 to 0x4203FFFF, although these addresses are not mapped by default to the device PCI address range.

Steps to be performed by the designer

Writing 1 to register 0x30C3C bit[15], during the device configuration after reset, prevents the device from responding erroneously to this PCI address range.

4.33 Addr64 Field in the PCI MSI Message Control Register Has No Effect

Type: Guideline
Ref #: GL-PCI-30
Relevant for: 88F5182-A1/A2

Description

The <Addr64> field (bit[23]) in the PCI MSI Message Control register (offset: 0x50) has no effect.

When this bit is set to 0 (Not capable) and the PCI MSI Message High Address register (offset: 0x58) is not set to 0, the 88F5182 PCI master will still issue transactions with 64-bit addresses.

Steps to be performed by the designer

Write the value of 0x0 to the MSI High Address register.

PCI Interface Restrictions

4.34 Write to PCI Access Control Size Registers

Type: Restriction
Ref #: RES-PCI-20
Relevant for: 88F5182-A1/A2

Description

When writing to PCI Access Control Size x registers (offset: 0x31E08, 0x31E18, 0x31E28, 0x31E38, 0x31E48, 0x31E58), either from the CPU or from an external master residing on the PCI Bus, a 32-bit write access should be performed (no byte or half word write access is permitted).

4.35 Simultaneous Peer-to-peer Traffic Deadlock

Type: Restriction
Ref #: RES-PCI-30
Relevant for: 88F5182-A1/A2

Description

A deadlock may be reached when forwarding peer-to-peer traffic simultaneously in both directions between the PCI Express port and a PCI port.

Workaround

Do not use simultaneous peer-to-peer traffic.

4.36 Aggressive Prefetch Read May Cross the BAR Boundary

Type: Restriction
Ref #: RES-PCI-60
Relevant for: 88F5182-A1/A2

Description

The PCI slave does not disconnect an aggressive prefetch read transaction when reaching the Base address register (BAR) boundary. The PCI slave continues prefetching read data regardless of the BAR boundary.

Workaround

Use either of the following workaround options:

- Do not map BARs consecutively.

  OR
- Make sure the Master does not initiate aggressive prefetch read transactions that pass the BAR boundaries.

4.37 PCI_AD[1:0] Wrong Address Value During IO Transaction

Type: Restriction
Ref #: RES-PCI-70
Relevant for: 88F5182-A1
Not Relevant for: 88F5182-A2

Description
When using the Internal PCI Arbiter, if the device initiates a PCI IO transaction to a not aligned address, the device generates the correct value for the CBE#[3:0] signals. However, the device may not set the correct decoded value to the AD[1:0] signals.

Workaround
Either:

- Use an external PCI arbiter.
  OR
- In the PCI Arbiter Control register (offset 0x31D00), set field <PD[6:0]>, bits[20:14], to 0x1 to prevent the internal PCI arbiter from parking on the device.

4.38 Incorrect Behavior of the <INS> Bit During CompactPCI HotSwap Board Extraction Operation

Type: Restriction
Ref #: RES-PCI-80
Relevant for: 88F5182-A1/A2

Description
The CompactPCI HotSwap specification allows the user to start a board extraction operation, and then stop it without completing the actual extraction of the board. This means that the user opened the handle switch, and then re-locked it, without extracting the board from the backplane.

When the switch is re-locked, the hardware should set the HotSwap Status and Control register <INS> bit to 1. This setting causes the PCI_ENUMn signal to be asserted, indicating to the host that an insertion operation is in progress.

The 88F5182 fails to set the <INS> bit during this sequence.

Steps to be performed by the designer
Complete the entire extraction process by physically removing the board, and then re-installing it in the backplane.

Serial-ATA Guidelines

4.39 Wrong Default Value to PHY Mode 4 Register Bits[1:0]

Type: Guideline
Ref #: GL-SATA-100
Relevant for: 88F5182-A1/A2

Description

Due to the wrong default value of the <PhyIntConfPara> field, bits[1:0], in the PHY Mode 4 Register, the OOB initialization sequence (Link initialization) may not succeed on rare occasions.

After completing the initialization sequence, the result of the OOB sequence can be observed per channel in the channel SStatus Register.

- Correct OOB results are: Gen1 - x113; Gen2 - x123;
- Incorrect OOB results are: Gen1 - other than x113; Gen2 - other than x123.

Steps to be performed by the designer

1. Set bits[1:0] in the PHY Mode 4 Register to 0x1 before starting the channel.
   AND
2. If the SStatus Register shows that there is a channel connection problem, restart the channel.

Note

Refer to GL#SATA-S12 for more details on link initialization.

4.40 PHY Mode 3 Register Configuration

Type: Guideline
Ref #: GL-SATA-110
Relevant for: 88F5182-A1/A2

Description

The default values of the PHY Mode 3 registers (offset: Port0: 0x82310, Port1: 0x84310) have to be modified by Read Modify Write as follows:

1. Write 0x0 to bits[4:2]
2. Write 0x0 to bit[20].
3. Write 0x55 to bits[30:23].

Steps to be performed by the designer

Using software, perform a Read Modified Write according to the following pseudo-code example:

i = Read Value of PHY MODE 3 Reg;

i = i & NOT(0x7F90001C);

i = i | 0x2A800000;

Store i to PHY MODE 3 Reg;

4.41 Using SATA II 3.0 Gbps Host with 1.5 Gbps Device

Type: Guideline
Ref #: GL-SATA-120
Relevant for: 88F5182-A1/A2

Description

When the Marvell® SATA II host is configured for 3.0 Gbps operation and connects to a device configures for 1.5 Gbps operation, occasionally it might fail to negotiate the link speed. In such a case, the host may wrongly try to establish a 3.0 Gbps link speed connection. This results in a situation where the operating system does not recognize that the device is present.

Steps to be performed by the designer

To use 1.5 Gbps SATA devices with the Marvell SATA II host, use the following steps during the SATA link initialization:

1. Perform an interface communication initialization sequence to establish communication by writing 0x1 to the <DET> field in the SControl register (SControl=0x301). This will force the host to send a COMRESET.
2. Allow link negotiation by clearing the <DET> field (writing 0x0 to that field).
3. Read the SStatus register a few times (for example, 200 times with the Marvell driver).
4. If the status is not 0x0, 0x113, or 0x123 on the last try, repeat steps 1–3 (for example, five times with the Marvell driver).
5. If the SStatus is not 0x0, 0x113, or 0x123 after five times of resetting the link, then set the maximum speed to 1.5 Gbps, by writing 0x0 to the <Gen2En> field, bit[7] in the Serial-ATA Interface Configuration register, and then write 0x1 to the <eATARst> field, bit[2] in the EDMA Command Register.
6. Repeat steps 1–3.
7. If the SStatus is still not 0x0 or 0x113, the driver views the link as inactive.

Fix:

None.

4.42 PHY Mode 1 Register Configuration

Type: Guideline
Ref #: GL-SATA-130
Relevant for: 88F5182-A1/A2

Description

The default value of the PHY Mode 1 registers has to be modified by performing Read Modify Write as follows: Write 0x2 to bits[31:30].

Steps to be performed by the designer

Using software, perform a Read Modified Write according to the following pseudo-code example:

i = Read Value of PHY MODE 1 register;

i = i & NOT(0xC0000000);

i = i | 0x80000000;

Store i to PHY MODE 1 register;

USB 2.0 Interface Guidelines

4.43 USB Calibration after Reset

Type: Guideline
Ref #: GL-USB-10
Relevant for: 88F5182-A1/A2

Description
Setting the calibration of the USB PHY must be done after reset, before enabling the USB interface.

Steps to be performed by the designer
Perform a Read-Modify-Write to the USB PHY internal register at offset 0x50420:

1. Set bit[13] to 0x1.
2. Set bits[6:3] to 0x8.

4.44 Reset of the USB Core via the USBCMD Register Bit <Rst> Clears the USB MODE Register

Type: Guideline
Ref #: GL-USB-20
Relevant for: 88F5182-A1/A2

Description
Reset of the USB core via <Rst> bit[1] in the USBCMD register (offset: 0x50140) causes a clear of the USBMODE register (offset: 0x501A8). This leaves the USB core in an undefined state (with neither Device nor Host defined).

All existing EHCI Host drivers (Linux, VxWorks) perform USB core reset during their initialization sequence, but they do not set the USBMODE registers (non EHCI compliant).

Steps to be performed by the designer
Configure bits[1:0] in the USBMODE register to Host/Device mode after each reset of the USB core.

4.45 USB PHY Configuration

Type: Guideline
Ref #: GL-USB-30
Relevant for: 88F5182-A1/A2

Description
Default values of the USB PHY registers have to be modified as follows:

1. USB PHY Rx Control register (offset: Port0: 0x50430, Port1: 0xA0430):
   Write 00 to bits[9:8] (

   Write 0 to bit[21]

   Write 00 to bits[27:26]

   Write 11 to bits[31:30]
2. USB PHY Test Group Control register (offset: Port0: 0x50450, Port1: 0xA0450):
   Write 0 to bit[15]
3. USB PHY IVREF Control register (offset: Port0: 0x50440, Port1: 0xA0440):
   Write 10 to bits[1:0]

Steps to be performed by the designer
Perform modifications to the above listed bits through software or TWSI serial initialization.

4.46 Vbus Support through GPIO

Type: Guideline
Ref #: GL-USB-40
Relevant for: 88F5182-A1/A2

Description

The USB core is a self-powered device, therefore the Vbus is not used in device mode for sensing the existence of a USB connection.

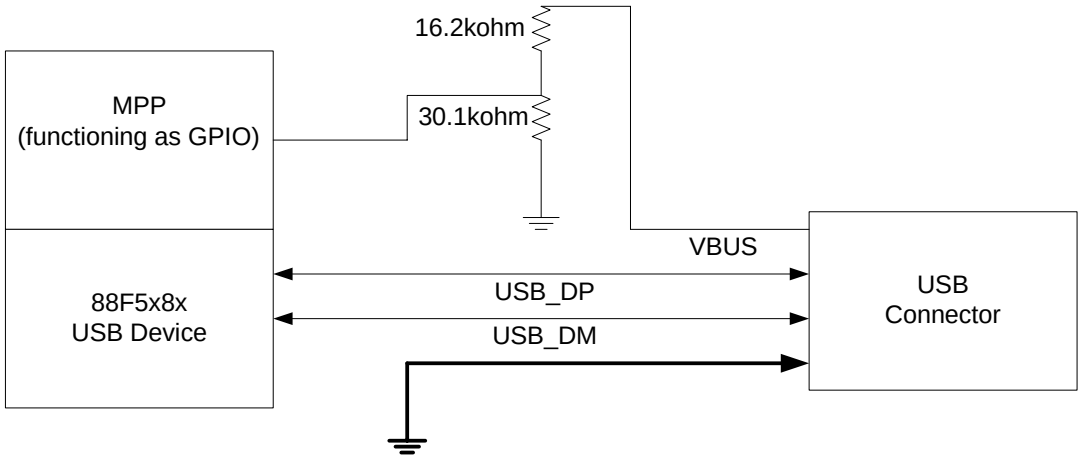
The USB 2.0 specification includes the following requirement: "When the host goes to power down and drops the VBUS to 0, the device must remove the pull-up resistor on the DP."

Steps to be performed by the designer

To support the above requirement the following is recommended:

- Connect the Vbus coming from the USB connector to an MPP pin selected to function as GPIO (input interrupt), through a voltage divider as described in Figure 1.
- Issue an interrupt each time the Vbus drops.
- Upon an interrupt write to the USB Power Control register (offset: 0x50400) bits[26:25] 2'b00 (the default value is 2'b11). This will remove the pull-up resistor on the DP.

Figure 1: USB VBUS Connection to GPIO



Note: Resistor values of the voltage divider may be different that what appear in the Figure 1. However, the ratio between the resistor values must remain the same.

4.47 Avoiding Three Consecutive CRC Errors on the USB Port when Working in HS Mode

Type: Guideline
Ref #: GL-USB-50
Relevant for: 88F5182-A1/A2

Description

An occasional CRC error on the bus is expected to be handled correctly by the system. However, when three consecutive CRC errors are generated, either when the device operates as a host or a device, the USB link may reset and cause reset of the USB port.

These CRC errors only occur if the USB port is set to work in HS mode.

Steps to be performed by the designer

To avoid the above scenario, set the USBMODE register (offset 0x501A8) bit[4] to 1, which activates Stream Disable mode.

4.48 Remote Wake-Up Recognition Failure

Type: Guideline
Ref #: GL-USB-60
Relevant for: 88F5182-A1/A2

Description

This guideline applies to the USB in Host mode.

The MV78100 does not recognize a remote wake up.

Steps to be performed by the designer

After writing the suspend bit, the software driver must wait at least 5 ms before writing the low power bit (clock disable). Without the 5 ms pause, when the clock starts, as a result of a remote wake up from the device, that remote wake up may not be recognized by the USB port.

4.49 PID Tracking Errors May Occur for an Active Endpoint

Type: Guideline
Ref #: GL-USB-70
Relevant for: 88F5182-A1/A2

Description

This guideline applies to the USB in Device mode.

Where only one endpoint of an endpoint pair is used and the other is inactive, if the unused endpoint is programmed to the default control type, this may result in data PID tracking errors for the active endpoint.

Steps to be performed by the designer

The unused endpoint type must be programmed to bulk.

4.50 Missed Resume Interrupt after Suspend in Host Mode

Type: Guideline
Ref #: GL-USB-80
Relevant for: 88F5182-A1/A2

Description

The host might miss an interrupt on a resume after a suspend. The port-change-control interrupt is not activated, and there is no port-change-toggle for the host to resume after being suspended.

Steps to be performed by the designer

In Suspend mode, the software should look for start of frames (SOFs). If SOFs are being generated then the port has resumed.

4.51 Inaccurate Squelch Levels in High-Speed Mode

Type: Guideline
Ref #: GL-USB-90
Relevant for: 88F5182-A1/A2

Description

Reception of data is qualified by the output of the transmission envelope detector. The receiver must disable data recovery when the amplitude of the differential voltage signal is less than 100 mV, and must not indicate squelch if the amplitude of the differential voltage signal is higher than 150 mV.

The transmission envelope detector is tested according to the *USB-IF Electrical Test Specification,* revision 1.3 EL_16 and EL_17.

Using the recommended setting would ensure:

- Squelch indication when the amplitude of the differential voltage signal is less than 100 mV (EL_16: Pass).
- Non-Squelch indication when amplitude of differential voltage signal is higher than 170 mV (EL_17: Waiver). EL_17 waiver is granted if the receiver does not indicate Squelch at ±50 mV of the 150 mV differential amplitude).

Steps to be performed by the designer

Default values of the USB PHY registers have to be modified by Read-Modify-Write as follows:

- USB Power Control register (offset: Port0: 0x50400, Port1: 0xA0400):
  bits[7:6] change to 0x1
- USB PHY Rx Control register (offset: Port0: 0x50430, Port1: 0xA0430):
  bits[7:4] change to 0x1
- USB PHY IVREF Control register (offset: Port0: 0x50440, Port1: 0xA0440):
  bits[5:4] change to 0x3
  bit[19] change to 0x0

4.52 Enable Fix for USB Host Compliance Electrical Test Plan—EL23

Type: Guideline
Ref #: GL-USB-100
Relevant for: 88F5182-A2

Description

To enable a design fix of *USB Host Compliance Electrical Test Plan—EL23*, a field in the register at offset 0x50360 needs to be modified.

Step to be performed by the designer

At offset 0x50360, use Read Modify Write to modify the default value of bits[14:8] to 0xC.

4.53 USB Full Speed—Receiving Packets with No EOP Indication

Type: Guideline
Ref #: GL-USB-110
Relevant for: 88F5182-A1/A2

Description

When working in Full Speed mode, if a packet is received immediately after a packet for which no EOP has been received, then this second packet is received as a corrupted packet. However, the SE0 portion of its EOP is recognized. This results in the receiver closing reception of the second packet and returning to the state where it is ready to receive the next packet. The third packet is then received as a normal packet.

Steps to be performed by the designer

When working in Device mode: None.

When working in Host mode: Detecting and handling the above scenario is done during the USB IRQ procedure, as follows:

- Check if the USB_STS register (offset: 0x50144) bit[1] (USB Error) is set to 1.
- Check if the USB device is attached—in the PORTSC1register (offset: 0x50184), bit[0] (CCS) is set to 1.
- Check if the USB port is disabled—in the PORTSC1register (offset: 0x50184), bit[2] (PE) is set to 0.
- Check if the USB device is in Full Speed mode—in the PORTSC1register (offset: 0x50184), bits[27:26] (PSPD) is set to 00.

The order in which the above steps are performed is not important.

Run the reset sequence on the USB port (depend on USB Host stack implementation).

4.54 USB High Speed—Receiving Packets with No EOP Indication

Type: Guideline
Ref #: GL-USB-120
Relevant for: 88F5182-A1/A2

Description

When working in High Speed mode, if a packet is received with no EOP, one of the following two scenarios occurs:

- The packet is received internally as a corrupted packet (that is, an Rx error is asserted) and the controller requests the packet again.
  OR
- The packet is received internally as a proper packet, and the controller checks it for CRC:
  - If the CRC check fails, the controller requests the packet again.
  - If the CRC check passes, the controller use the packet as if there was no error.

In both scenarios, the controller recovers from this error situation.

Steps to be performed by the designer

None.

USB 2.0 Interface Restrictions

4.55 USB Isochronous Mode

Type: Restriction
Ref #: RES-USB-10
Relevant for: 88F5182-A1/A2

Description

For USB Isochronous mode support, contact a local Marvell® Field Applications Engineer or representative.

Workaround

None.

4.56 USB Electrical Test Plan EL15 (Reception Reliability/Vcommon Range Restriction)

Type: Restriction
Ref #: RES-USB-160
Relevant for: 88F5182-A1/A2

Description

When receiving data in high-speed mode, the differential receiver will reliably receive signals in the presence of a common mode voltage component (V_{HSCM}) of up to 270 mV (refer to the *Universal Serial Bus Specification*, Revision 2.0).

Workaround

None.

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